Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	11	mukunoki-toshio.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 10:58
S2	280	sugimoto-akira.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 10:58
S3	72	ozeki-takao.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 11:02
S4	1	S1 and S2 and S3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 10:58
S5	791431	matsushita.as.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 11:02
S6	2	S2 and S5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 11:02
S7	2	S3 and S5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 11:03
S8	6	(("6414890") or ("10302498")).PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/17 12:32

S9	3309	365/201.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 12:38
S10	504	365/185.01.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 12:41
S11	8857	"memory cell" and (stress burn-in)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 12:40
S12	2923	"memory cell" same (stress burn-in)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 12:40
S13	523	365/185.26.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 12:41
S14	45	S13 and S12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 14:34
S15	376	S12 and S9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 12:43
S18	1116	("floating gate" floating-gate) and S12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 14:35

S19	185864	(("silicon oxide" silicon-oxide) and ("silicon nitride" silicon-nitride)) or (oxide-nitride-oxide ONO)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 12:50
S20	381	S18 and S19	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 12:51
S21	153	S18 and (fuse "MIS transistor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 09:40
S22	499	S12 and (fuse "MIS transistor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 12:53
S23	45	S15 and S18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 13:38
S24	681	"memory cell" same "burn-in"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 14:34
S25	57	("floating gate" floating-gate) and S24	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/18 11:44
S26	24	S25 and S19	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 14:36

S27	21	S26 and fuse	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 14:37
S29	216	S24 and S9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/17 15:05
S30	280	stress$3 near20 ((sample or dummy or reference) adj3 cell$1)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/18 11:44
S31	2923	"memory cell" same (stress burn-in)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 09:40
S32	1116	("floating gate" floating-gate) and S31	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 09:40
S33	186320	(("silicon oxide" silicon-oxide) and ("silicon nitride" silicon-nitride)) or (oxide-nitride-oxide ONO)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 09:40
S34	381	S32 and S33	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 09:40
S35	66	S34 and (fuse "MIS transistor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 10:47

S38	732	("memory cell") and ((dummy or sampl$3) near2 cell) and ("floating gate" floating-gate)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 15:58
S39	170	S33 and S38	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 11:00
S40	25	S39 and (fuse "MIS transistor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 11:00
S41	23	((dummy or sampl$3) near2 cell) same (low$3 adj (resistance or resistivity)) same (memory adj cell)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 11:48
S43	80	((dummy or sampl$3) near2 cell) same (low$3 adj (resistance or resistivity))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 11:48
S44	2	((dummy or sampl$3) near2 cell) same (low$3 adj resistivity)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 11:49
S45	4	((dummy or sampl$3) near2 cell) same (high$2 adj conductivity) same (memory adj cell)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 12:52
S46	8	((dummy or sampl$3) near2 cell) same (high$2 adj conductivity)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 12:57

S47	1427	((dummy or sampl$3) near2 cell) same (fuse switch "MIS transistor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 12:57
S48	114	((dummy or sampl$3) near2 cell) same (fuse "MIS transistor")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 14:39
S49	50	"MIS transistor" same (shortcircuit$3 short-circuit$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 14:56
S50	6691	"memory cell" same ((switch MIS) transistor$2) same parallel	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 14:57
S51	1740	("memory cell") same ((switch MIS) transistor$2) same (parallel near2 connect$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 15:00
S52	1798	("memory cell") with (parallel near2 connect$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 15:00
S53	23	S52 same ((switch MIS) adj transistor$2)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 15:07
S57	522	"memory cell" same (referenc$3 adj circuit)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 15:16

S58	40	"memory cell" same ((referenc$3 adj circuit) with threshold)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 15:20
S59	9	"memory cell" same ((referenc$3 adj circuit) with (writ$3 and eras$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 15:20
S60	520	("memory cell") and ((dummy or sampl$3) near2 cell) and (source adj line$2)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 16:00
S61	170	("memory cell") same ((dummy or sampl$3) near2 cell) same (source adj line$2)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/22 10:39
S62	2	("memory cell") same ((dummy or sampl$3) near2 cell) same (equalization adj circuit)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/22 10:43
S63	6	("memory cell") same (equalization adj circuit) same (read near2 circuit)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/22 11:08
S64	143	("memory cell") same (equalization adj circuit) same (data)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/22 11:08